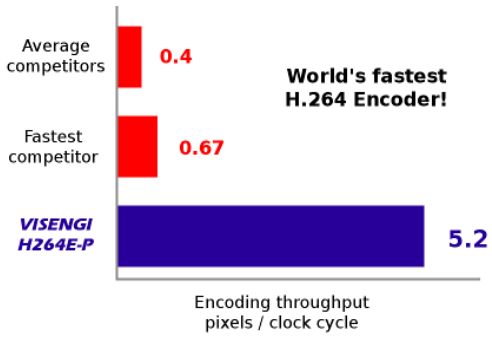
VISENGI
Hardware & Software Engineering

H264 Encoder IP core
Product Brief

VISENGI's H.264 Encoder IP core has been engineered to be the highest throughput standards-compliant hardware video compressor.

It is currently the only **H.264 Encoder IP core** delivering **8K 30 Hz on mid-range FPGAs** and **UltraHD 4K 60 Hz on low-range FPGAs**.



VISENGI offers two encoder variants to meet different targets of: features, resource usage, and compression:

- **H264E-I**: Compliant with **CAVLC 4:4:4 Intra Profile** (all frames are keyframes): the IP core is **smaller** but yields less compression. It requires **no external memory**.

- **H264E-P**: Compliant with **High 4:4:4 Predictive Profile**: the IP core is **larger** but offers a significantly **better compression**.

On top of this, VISENGI's H.264 Encoder is able to **encode 32 input video streams in parallel**, each with a different set of parameters, resolution, ...

Check the latest product information at:

http://visengi.com/products/h264_encoder

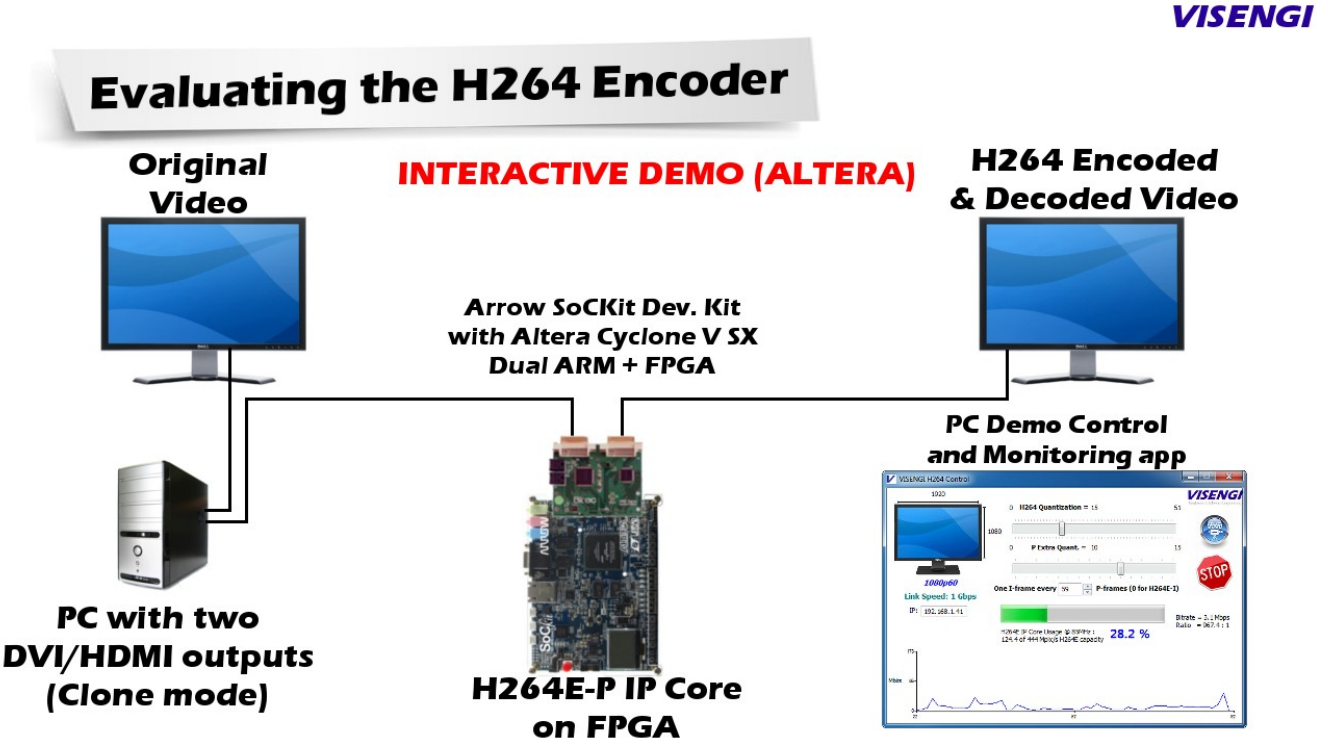
Request your free evaluation at: info@visengi.com

Parameter	Value
H.264 Profile	High 4:4:4 Predictive (H264E-P) CAVLC 4:4:4 Intra (H264E-I)
Throughput	**5.2 pixels/cycle (constant)**
Max. resolution	- Xilinx Artix-7 4K 60 fps - **Xilinx Zynq 7030 8K 30 fps** - Altera Cyclone V 4K 60 fps - **Altera Arria 10 8K 30 fps**
User parameters	- Constant Bitrate (CBR) in Kbps - Constant Quality (VBR) in QP ratio
Max. framesize	16Kpix by 16Kpix
Max. framerate	64K fps
Latency	Lowest (16 video lines always)
Multiple inputs	**Up to 32 input streams in parallel**
Color handling	4:4:4 pipeline, for maximum fidelity
Input formats	YCbCr and RGB (≤ 24bpp) 4:4:4 / 4:2:2 / 4:2:0
IP core interfaces	**Industry Standard AXI Interfaces:** - AXI-Lite configuration - AXI3/4 and AXI4-Stream data I/O
AXI3/4 capabilities	Embedded DMA (directly connect to memory controller)
AXI4-Stream capabilities	Connect to row-wise pixel sources (HDMI/DVI, image sensors, etc)
External components	- **No CPU required** - External memory for H264E-P only
Instantiation	**Easy drag'n'drop IP block for Xilinx Vivado Block Design GUI and Altera Quartus Qsys GUI**
Resource usage	Xilinx: 54K LUTs / 32 DSPs Altera: 35K ALMs / 32 DSPs ** Smaller versions available*
FPGA ARM SoC support	Deliverables include: - Linux kernel module driver (H264E as HW peripheral) source code - Linux HW H264 sample application source code - Devicetree + Kernel update instructions
Technical Support	1 year technical support included with purchase. Extended time packages available.

Download the free H264E IP blocks and Quick Start Guide (PDF) to instantiate VISENGI's H264 Encoder into your design today!

For Xilinx Vivado Block Design GUI: http://visengi.com/docs/VISENGI_H264E_P_Xilinx.zip
For Altera Quartus Qsys GUI: http://visengi.com/docs/VISENGI_H264E_P_Altera.zip

Try the full evaluation on your premises with our H264 Encoder **1080p60 interactive demo** running on a Cyclone V SoC:



Requires one Arrow SoCkit board plus a Bitec or Terasic HSMC-DVI card.
As simple as flashing the evaluation file to a MicroSD.
Remotely control the H264 IP core's encoding parameters through a Windows application.

Or try **H.264 Network Streaming Demo** for AvNet PicoZed Zynq 7030, or for Arrow SoCkit

Click on "Request Quotation" on the product page
http://visengi.com/products/h264_encoder
to receive full pricing, documentation, and evaluation information.

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